GRIDBYTE™
MULTI-DIMENSIONAL THINKING

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Title: MOS IC Design For Manufacturing (DFM) Below 90nm, A Mixed-Signal Perspective
White Paper: GridByte-WP2006-01 (rev. 02)
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The need for robust mixed-signal DFM techniques increases exponentially as MOSFET features go well below the 90nm mark. For example, at 45nm, maskset costs exceeding $9 million coupled with engineering costs make it necessary to incorporate DFM thinking into the entire production process—system-level and architecture, design, layout and packaging of mixed signal ICs. Perhaps DFM is the single problem that the semiconductor industry must solve immediately because the cost of not having proactive solutions is already too high for small and large companies.

Traditionally, mixed-signal design teams have considered DFM in the context of yield enhancement. Sometimes, this is an exercise separate from initial design. When IC failures requiring respins occur, the explanations are often speculative because of poor insight into the complex IC. Moreover, the lines between mixed-signal and digital no longer exist. Many high-speed digital circuits behave like mixed-signal elements. Thus the roles of mixed-signal DFM are much larger than the traditional big D, little A.

Proactive DFM requires even greater collaboration between EDA tool vendors, fabrication vendors and IC design teams. In this paper, we provide bullet points to encourage critical new thinking that leads the design community to more proactive DFM solutions. DFM is a much bigger issue than yield enhancement. Incorporation of DFM thinking determines whether an IC project succeeds or fails.

The core issues at the center of any discussion on DFM are identified below in no particular order. These thoughts are a front-end based approach.

- As active device modeling complexity increases—designs must use models with tight binning. Devices structures must use smaller distributed structures (e.g., MOSFETS in parallel) to produce tighter correlations between models and physical structures.
- Passive devices (resistors, capacitors, inductors, special structures) show stronger non-linear dependencies on terminal voltages, back-gate voltages and temperature. 3D non-linear effects need to be modeled. Binning models must be included for passive devices.
- Device models must simultaneously account for small- and large-signal noise and distortion effects.
- Designs need to be exercised at the endpoints of the modeling space. There is widespread use of Monte-Carlo methods. However, our experience shows limited value in many mixed-signal projects. End-point simulation should not be confused with Monte-carlo simulations.
- Designs in most cases simply need to be simulated! Our experience in trouble-shooting ICs shows that a large number of failures are due to limited exercise of the simulation space. “The purpose of simulation,” to paraphrase an old mentor, “is to find out where our circuits break.” Too often we find that core simulations are not done.
- High voltage induced hot-electron degradation, ballistic transport and dynamic breakdown shorten device lifetime. “High-voltage” is 2.5V at 90nm nodes. These effects necessitate greater use of Safe Operating Area (SOA) modeling techniques for static and dynamic simulation.
- Interface design needs greater attention. When dealing with IP blocks (black-box, or otherwise) the interfaces are often inadequately simulated. Some obvious problems such as incorrect node connections may be easy to see. However, some insidious parasitic and loading problems cause many yield loses that are hard to debug. Notably, interface design usually is most problematic when mixed-voltage elements cause lower-voltage elements to fail due to over-voltage effects.

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- Designers need to consider active clamps and other "brute-force" techniques to limit and control node voltages.
- Localized heating effects lead to tunneling phenomena that shorten lifetimes of devices. Localized heating leads to delamination effects for some high-current devices.
- RF coupling and EMI radiation effects create unexplained IC phenomena. In some test cases, we see complex phenomena that are difficult to debug.
- High metallization stacks (6 to 8) make it difficult to debug many ICs. Thus routing needs to be considered in the context of making debugging easier. Some innovative techniques include "routing streets," non-overlap of active structures, etc.
- Voltage drops on bias and interconnect lines cause large static and dynamic drops that degrade performance.
- Current densities need to be derrated significantly to increase the life-spans of interconnect and active devices.
- Design complexity requires greater use of digital control elements in conjunction with distributed analog test multiplexers to isolate/calibrate mixed-signal performance. Digital trimming methods are more robust than fuse-based trim methodologies. However, digital methods typically require a host or on-board digital engine. Sometimes, the pin-count must be increased to allow greater digital controllability and calibration. Further, digital calibration needs to be considered for mission-mode.
- Parasitic extraction and re-simulation are necessary. Many mixed-signal designs are not re-simulated with accurate parasitic elements. However, DFM dictates attention to parasitic simulation as a necessary component of design. The flip-side is that complex parasitic simulations are compute-resource intensive. Thus the design community continues to look to the EDA community for a 10× leap in simulation efficiencies of core spice-like simulators.
- Circuit layout is a significant component of the DFM equation. Most ICs pass all design rules … yet exhibit large yield losses because a whole host of issues (e.g., contact current handling capability for IR and electromigration, coupling issues, static and dynamic conductor sizing, etc) are routinely ignored. In general, a custom mixed-signal layout requires huge learning strides. In many organizations, risk mitigation forces planners to use scarce design resources for layout of sub-90nm IC blocks. These trends may lead to better layouts, but they also limit the amount of time the designer can spend validating designs.
- Designers need to carefully consider structures for current-crowding, crowbar effects and other failure modes that result from the shapes of conductive geometries.
- Mixed-signal layout teams must become versed in the hundreds of complex design rules and their subsets. As L. Stok points out in his paper titled *Prescriptive CAD*, "… design rules have become difficult to formulate, impossible to code, unique to specific environments, and prone to error."[1]
- As device packing density increases, we observe many strange effects. Many are due to substrate coupling and latchup effects. Many can be identified by a careful review. Package stress factors have also been reported widely as affecting critical performance. For example, voltage induced stresses reportedly lead to large shifts in bandgap voltages.
- Circuit design techniques need to evolve to ensure DFM robustness. Mixed-signal designs need to use common building blocks; e.g., all amplifiers on the IC should be replicas of a single design. The designs should use multiple programmability options for current drive, power consumption and stability. This common-element based design style

[1] Richard Goering, "IBM EDA director calls for 'prescriptive CAD," EE Times, http://www.eetimes.com/showArticle.jhtml;?articleID=198701495, 13 APR 2007.

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reduces the complexity of debugging large mixed-signal ICs—i.e., the philosophy is that common errors are easier to identify and debug.

- Mixed-signal designers must expand design considerations far beyond electrical considerations. This is certainly not to suggest that the variables they consider are not already huge. The problems just get bigger.
- Designs need to utilize multiple-signal-path architectures with block bypass. This allows board-level compensation and external bypass of on-chip blocks. At the end of the day, even a partially successful mixed-signal IC may yield a successful product. On this note, block bypass elements must be designed to ensure that analog signal fidelity is preserved.
- Design must continue to exploit fully differential architectures—we observe a large number of pseudo-differential designs that have no performance advantages over single-ended designs. Our prevailing attitude must continue to stress that it is always possible to make a signal path fully differential.
- Some design techniques applied to mixed-signal ICs include parallelism and other novel partitioning schemes.

Finally, the sub-90nm breed of an IC project leader must become part of the entire development cycle. This means that they need to become an integral part of the decisions during each phase; i.e., specification, architecture, design and layout, production test and ramp up. Their project matrix must include a credible risk matrix that includes DFM considerations at all levels.

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